CLAIMS

What is claimed is:

1. A method comprising:

generating an enable signal in response to a digital address strobe signal and a digital address select signal to activate the enable signal prior to receipt of an address packet; and

providing a flow-through path from an address pin to a chipset for a first component of the address packet in response to the enable signal, such that the first component of the address packet is provided to the chipset once the address packet appears on the address pin to expedite initiation of decoding of the address packet by the chipset.

2. The method of claim 1, wherein the generating of the enable signal further comprises:

feeding the digital address select signal as a clock pulse input of a first gate including a feed-back inverter coupled between an input and an output of the first gate;

feeding the digital address strobe signal as a clock pulse input of a second flip-flop including a feed-back inverter coupled between an input and an output of the second flip-flop; and

performing an exclusive-OR operation on an output of the first gate and an output of the second gate to generate the enable signal.

3. The method of claim 1, wherein the generating of the enable signal further comprises:

receiving an analog source synchronous strobe signal on an address strobe pin; and

converting the analog address strobe signal to a digital address strobe signal as the digital address strobe signal using a differential amplifier and a reference voltage.

4. The method of claim 1, wherein the generating of the enable signal, further comprises:

receiving an analog common clock protocol signal on an address select pin;

converting the analog common clock protocol signal into a digital common clock protocol signal using a differential amplifier and a reference voltage;

feeding the digital common clock protocol signal as an input to a first gate and a common clock signal as a clock pulse input of the first gate to generate a flopped address select signal at an output of the first gate; and

feeding the flopped address select signal to an input of an inverter to generate the digital address select signal at an output of the inverter.

5. The method of claim 1, further comprising:

deactivating the enable signal in response to the detection of a transition in the digital address strobe signal; and

reactivating the enable signal, prior to receipt of a next address packet, in response to the detection of a transition in the digital address select signal.

6. The method of claim 5, wherein deactivating the enable signal further comprises:

detecting a falling signal transition of the digital address strobe signal; and

driving the enable signal high to disable the enable signal.

7. The method of claim 5, wherein reactivating the enable signal further comprises:

detecting a falling signal transition of the digital address select signal; and

driving the enable signal low to activate the enable signal prior to receipt of the next address packet.

8. The method of claim 1, wherein the enable signal is an active low signal, such that during reset of the enable signal, the enable signal is active prior to receipt of the address packet.

9. The method of claim 1, further comprising:

providing the second component of the digital address packet to the chipset in response to the digital address strobe signal, such that the chipset can complete decoding of the address packet.

10. The method of claim 1, wherein prior to providing the flow-through path, the method comprises:

receiving an address packet on an address pin for data requested from a processor on a system bus, the address packet having a first component describing a transaction type of the address packet and a second component describing attributes of the address packet.

11. An address receiver, comprising:

a flow-through circuit to generate an enable signal in response to a digital address strobe signal and a digital address select signal to activate the enable signal prior to receipt of an address packet; and

a flow-through gate having a digital address packet and the enable signal as inputs, the flow-through gate providing a first component of the digital address packet to a chipset in response to the enable signal once the digital address packet appears on the address pin,

thereby providing a flow through path from the address pin to the chipset for the first component of the digital address packet to expedite initiation of decoding of the address packet by the chipset.

12. The address receiver of claim 11, wherein the flow-through circuit further comprises:

a first gate including a feed-back inverter coupled between an input and an output of the first gate and the digital address select signal as a clock pulse input of the first gate;

a second gate including a feed-back inverter coupled between an input and an output of the second gate and the digital address strobe signal as a clock pulse input of the second gate; and

an exclusive-OR gate having an output of the first gate and an output of the second gate as inputs to generate the enable signal as an output.

13. The address receiver of claim 11, further comprising:

an input differential amplifier to compare an address packet received on an address pin for a data request against a reference voltage and generate a digital address packet, the digital address packet having a first component describing a transaction type of the address packet and a second component describing attributes of the address packet.

14. The address receiver of claim 11, further comprising:

a non flow-through gate having the digital address packet and a digital address strobe signal as inputs and providing the second component of the digital address packet to the chipset in response to the digital address strobe signal, such that the chipset can complete decoding of the address packet.

15. The address receiver of claim 14, wherein the non flow-through gate is a data flip-flop, the first gate is a data flip-flop and the third second gate is a data flip-flop.

16. The address receiver of claim 11, further comprising:

a first differential amplifier to compare a common clock protocol signal received on an address select pin against a reference voltage and generate a digital common clock protocol signal;

a first gate to receive the digital common clock protocol signal as an input and a common clock signal as a clock pulse input and generate a flopped address select signal at an output of the first gate; and

an inverter to receive the flopped address select signal and generate the digital address select signal at an output of the inverter for input to the flow-through circuit.

17. The address receiver of claim 14, wherein the non flow-through gate is a data flip-flop and the first gate flip-flop is a data flip-flop.

18. The address receiver of claim 11, further comprising:

a second differential amplifier to compare an analog address strobe signal received on an address strobe pin against a reference voltage and generate the digital address strobe signal.

19. The address receiver of claim 11, wherein the flow-through gate is an active low enabled latch.

20. A memory controller comprising:

a chipset coupled to the memory by a memory bus;

a system bus coupling a processor to the chipset, the chipset to decode an address packet on the system bus for data requested by the processor from the memory, wherein the system bus includes a source-synchronous address receiver including:

a flow-through circuit to generate an enable signal in response to a digital address strobe signal and a digital address select signal to activate the enable signal prior to receipt of an address packet;

a flow-through gate having a digital address packet and the enable signal as inputs, the flow-through gate to provide the first component of the digital address packet to a chipset in response to the enable signal once the digital address packet appears on an address pin, thereby providing a flow through path from the address pin to the chipset for the first component of the digital address packet to expedite initiation of decoding of the address packet by the chipset.

21. The memory controller of claim 20, further comprising:

a non flow-through gate having the digital address packet and the digital address strobe signal as inputs and providing the second component of the digital address packet to the chipset in response to the digital address strobe signal, such that the chipset can complete decoding of the address packet.

22. The memory controller of claim 20, wherein the flow-through circuit further comprises:

a first gate including a feed-back inverter coupled between an input and an output of the first gate and the digital address select signal as a clock pulse input of the first gate;

a second gate including a feed-back inverter coupled between an input and an output of the second gate and the digital address strobe signal as a clock pulse input of the second gate; and

an exclusive-OR gate having an output of the first gate and an output of the second gate as inputs to generate the enable signal as an output.

23. The memory controller of claim 20, wherein the flow through circuit is to deactivate the enable signal in response to the detection of a transition in the digital address strobe signal and to reactivate the enable signal, prior to receipt of a next address packet, in response to the detection of a transition in the digital address select signal.

24. The memory controller of claim 20, further comprising:

an input differential amplifier to compare the address packet received for the data request on the address pin against a reference voltage and generate a digital address packet, the digital address packet having the first component describing an address transaction type and the second component describing attributes of the address;

a first differential amplifier to compare an analog common clock protocol signal received on an address select pin against a reference voltage and generate a digital common clock protocol signal;

a first gate to receive the digital common clock protocol signal as an input and a common clock signal as a clock pulse input and generate a flopped address select signal at an output of the first gate; and

an inverter to receive the flopped address select signal and generate the digital address select signal at an output of the inverter for input to the flow-through circuit.

25. The memory controller of claim 24, wherein the first gate is a data flip-flop.

26. The memory controller of claim 20, further comprising:

a second differential amplifier to compare an analog source synchronous strobe signal received on an address strobe pin against a reference voltage and generate the digital address strobe signal.

27. The memory controller of claim 20, wherein the flow-through gate is an active low enabled latch.

28. The memory controller of claim 21, wherein the non flow-through gate is a data flip-flop.